

WHAT IS CLAIMED IS:

- 1 1. A method for fabricating a semiconductor device
- 2 comprising the steps of:
- 3 forming a lower wiring layer on a semiconductor
- 4 substrate;
- 5 coating two or more layers of dielectric films over
- 6 the lower wiring layer;
- 7 forming a via hole and a groove through the
- 8 dielectric films; and
- 9 forming an upper wiring layer in the groove and a
- 10 via in the via hole to connect the lower wiring layer with
- 11 the upper wiring layer,
- 12 wherein the maximum process temperature $T_{process_max}$
- 13 after forming the dielectric films is determined using
- 14 following inequality (1):
- 15
$$(\alpha - \alpha'_{die1}) \frac{E}{1-\nu} (T_{process_max} - T) \leq A$$
- 16 (1),
- 17 where A represents critical stress value near the
- 18 via, which is predetermined as a critical value causing
- 19 voids near the via by a thermal treatment after forming the
- 20 dielectric films,
- 21 α represents a thermal expansion coefficient of the
- 22 via and the upper wiring layer;
- 23 α'_{die1} represents an average thermal expansion
- 24 coefficient of the dielectric films calculated with their
- 25 relative thickness;

26 E represents an elastic coefficient of the via and
27 the upper wiring layer;

28 ν represents a Poisson's ratio of the via and the
29 upper wiring layer; and

30 T represents a stress relaxation temperature of
31 the via and the upper wiring layer.

1 2. A method for fabricating a semiconductor device
2 according to Claim 1,

3 wherein the upper wiring layer and the via are made
4 of metal.

1 3. A method for fabricating a semiconductor device
2 according to Claim 2,

3 wherein the upper wiring layer and the via are
4 made of copper, and

5 the maximum process temperature is determined
6 according to the inequality (1) using $T=300\text{ }^{\circ}\text{C}$ and $A=200$
7 MPa.

1 4. A method for fabricating a semiconductor device
2 according to Claim 2,

3 wherein the upper wiring layer and the via are
4 made of copper, and

5 the maximum process temperature $T_{process_max}$ is equal
6 to or lower than $450\text{ }^{\circ}\text{C}$.

1 5. A method for fabricating a semiconductor device

2 comprising the steps of:

3 forming a lower wiring layer on a semiconductor
4 substrate;

5 coating one or more layers of dielectric films over
6 the lower wiring layer;

7 forming a via hole and a groove through the
8 dielectric films; and

9 forming an upper wiring layer in the groove and a
10 via in the via hole to connect the lower wiring layer with
11 the upper wiring layer,

12 wherein combination of materials of the dielectric
13 films and relative thickness of the dielectric films are
14 determined based on α'_{diel} calculated by following
15 inequality (2):

$$16 \quad (\alpha - \alpha'_{diel}) \frac{E}{1 - \nu} (T_{process_max} - T) \leq A \quad (2),$$

18 where A represents critical stress value near the
19 via, which is predetermined as a critical value causing
20 voids near the via by thermal treatment after forming the
21 upper wiring layer,

22 α represents a thermal expansion coefficient of the
23 via and the upper wiring layer;

24 α'_{diel} represents an average thermal expansion
25 coefficient of the dielectric films calculated with their
26 relative thickness;

27 E represents an elastic coefficient of the via and
28 the upper wiring layer;

29 ν represents a Poisson's ratio of the via and the
30 upper wiring layer;

31 $T_{process_max}$ represents maximum process temperature of
32 the semiconductor device after forming the upper wiring
33 layer; and

34 T represents a stress relaxation temperature of
35 the via and the upper wiring layer.

1 6. A method for fabricating a semiconductor device
2 according to Claim 5,

3 wherein the upper wiring layer and the via are made
4 of metal.

1 7. A method for fabricating a semiconductor device
2 according to Claim 6,

3 wherein the upper wiring layer and the via are
4 made of copper, and

5 the combination of materials of the dielectric
6 films and the relative thickness of the dielectric films
7 are determined based on α'_{diel} calculated by the inequality
8 (2) using $T=300\text{ }^{\circ}\text{C}$ and $A=200\text{ MPa}$.

1 8. A method for fabricating a semiconductor device
2 according to Claim 6,

3 wherein the upper wiring layer and the via are

9. A semiconductor device comprising:

- a lower wiring layer formed on a semiconductor substrate;
- two or more layers of dielectric films formed over the lower wiring layer;
- a via hole and a groove provided through the dielectric films;
- an upper wiring layer formed in the groove; and
- a via formed in the via hole to connect the lower wiring layer with the upper wiring layer,

wherein the maximum process temperature $T_{process_max}$ after forming the dielectric films or materials of the dielectric films and relative thickness of the dielectric films are determined using following inequality (3):

$$(\alpha - \alpha'_{diel}) \frac{E}{1 - \nu} (T_{process_max} - T) \leq A \quad (3),$$

where A represents critical stress value near the via, which is predetermined as a critical value causing voids near the via by a thermal treatment after forming the dielectric films,

α represents a thermal expansion coefficient of the via and the upper wiring layer;

α'_{diel} represents an average thermal expansion

24 coefficient of the dielectric films calculated with their
25 relative thickness;

26 E represents an elastic coefficient of the via and
27 the upper wiring layer;

28 ν represents a Poisson's ratio of the via and the
29 upper wiring layer; and

30 T represents a stress relaxation temperature of
31 the via and the upper wiring layer.

1 10. A semiconductor device according to Claim 9,
2 wherein the upper wiring layer and the via are made
3 of metal.

1 11. A semiconductor device according to Claim 10,
2 wherein the upper wiring layer and the via are
3 made of copper, and
4 the maximum process temperature is determined
5 according to the inequality (1) using $T=300\text{ }^{\circ}\text{C}$ and $A=200$
6 MPa.

1 12. A semiconductor device according to Claim 10,
2 wherein the upper wiring layer and the via are
3 made of copper, and
4 the maximum process temperature $T_{\text{process_max}}$ is equal
5 to or lower than $450\text{ }^{\circ}\text{C}$.

1 13. A semiconductor device according to Claim 9,

2 at least one layer of the dielectric films is made
3 of ladder-oxide.

1 14. A semiconductor device according to Claim 13,
2 at least one layer of the other dielectric films is
3 made of SiC.